In The Claims

1. (Currently Amended) A metal oxide semiconductor (MOS) device comprising:

a semi-conducting substrate having source and drain regions;

a gate dielectric layer of less than 100 Å thickness on said semi-conducting substrate; and

a gate formed of a metal ~~selected from the group consisting of~~ comprising Re ~~and Rh~~ on top of said gate dielectric layer.

2. (Original) A metal oxide semiconductor device according to claim 1, wherein said gate dielectric layer having a thickness of less than 50 Å.

3. (Original) A metal oxide semiconductor device according to claim 1, wherein said gate dielectric layer is formed of a material selected from the group consisting of SiO_2, nitrided SiO_2, Si_3N_4, metal oxides and mixtures thereof.

4. (Original) A metal oxide semiconductor device according to claim 1, wherein said gate dielectric layer is formed of a material selected from the group consisting of Al_2O_3, HfO_2, ZrO_3, Y_2O_3, La_2O_3 and mixtures thereof including silicates and nitrogen additions.

5. (Original) A metal oxide semiconductor device according to claim 1, wherein said dielectric layer is formed of SiO_2.

6. (Canceled)

7. (Original) A metal oxide semiconductor device according to claim 1, wherein said semi-conducting substrate is p-type or n-type.

8. (Original) A metal oxide semiconductor device according to claim 1, wherein said semi-conducting substrate is formed of a material selected from the group consisting of silicon, SiGe, SOI, Ge, GaAs and organic semiconductors.

9. (Original) A metal oxide semiconductor device according to claim 1, wherein said semi-conducting substrate is formed of silicon.

10. (Currently Amended) A field effect transistor (FET) comprising:

a semi-conducting substrate having at least one source and one drain region;

a gate dielectric layer of less than 100 Å thickness on the semi-conducting substrate; and

a gate formed of a metal ~~selected from the group consisting of~~ comprising Re ~~and Rh~~ on top of the gate dielectric layer.

11. (Original) A field effect transistor according to claim 10, wherein the gate dielectric layer has a thickness of less than 50 Å.

12. (Original) A field effect transistor according to claim 10, wherein said gate dielectric layer is formed of a material selected from the group consisting of SiO_2, nitrided SiO_2, Si_3N_4, metal oxides and mixtures thereof.

13. (Original) A field effect transistor according to claim 10, wherein said gate dielectric layer is formed of a material selected from the group consisting of Al_2O_3, HfO_2, ZrO_3, Y_2O_3, La_2O_3 and mixtures thereof including silicates and nitrogen additions.

14. (Original) A field effect transistor according to claim 10, wherein said semi-conducting substrate is p-type or n-type.

15. (Original) A field effect transistor according to claim 10, wherein said semi-conducting substrate is formed of a material selected from the group consisting of silicon, SiGe, SOI, Ge, GaAs and organic semiconductors.

16. (Original) A field effect transistor according to claim 10, wherein said semi-conducting substrate is formed of silicon and said gate dielectric layer is SiO_2.